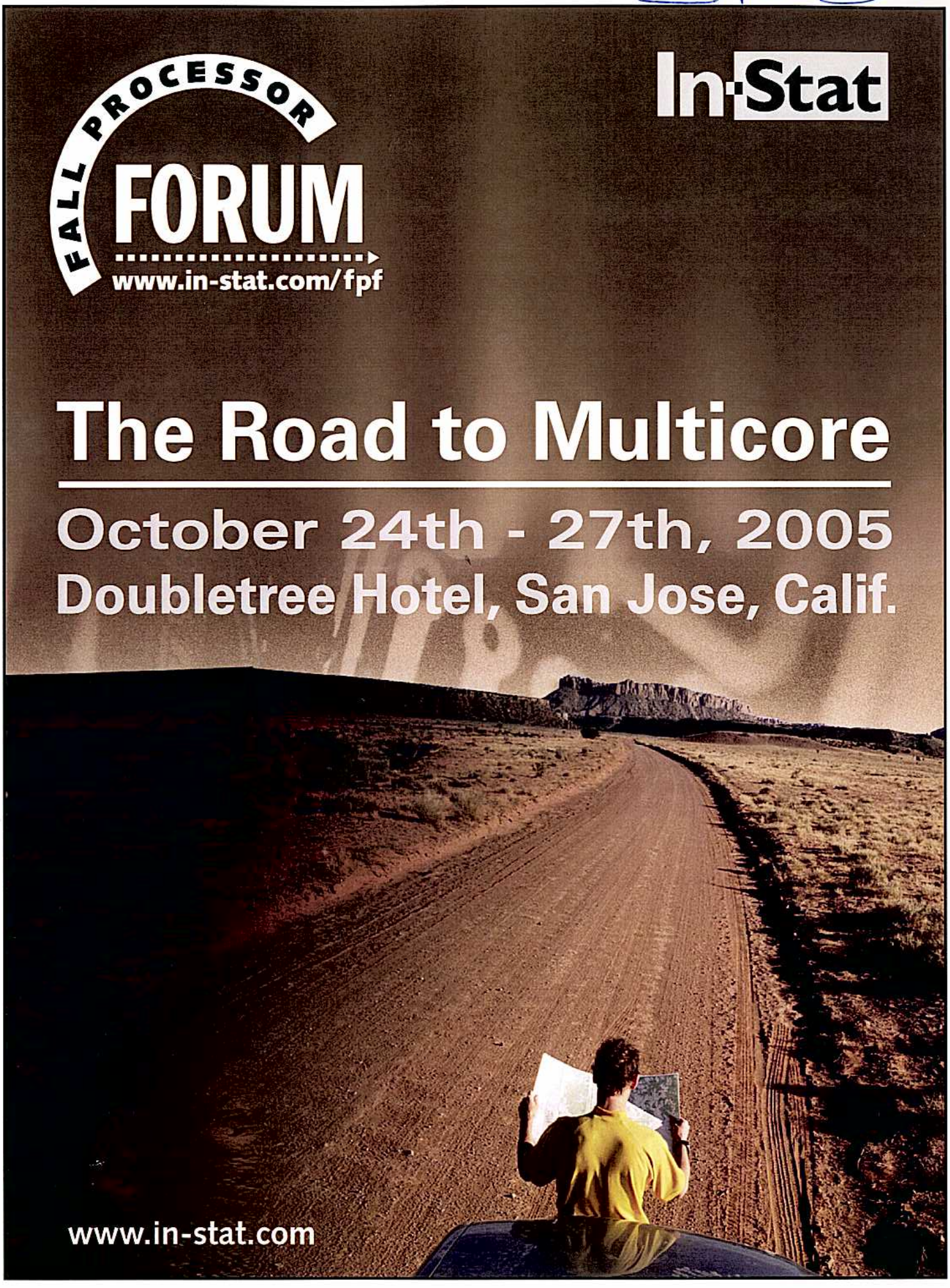
FALL PROCESSOR
FORUM
www.in-stat.com/fpf
In-Stat
The Road to Multicore
October 24th - 27th, 2005
Doubletree Hotel, San Jose, Calif.
www.in-stat.com

Dear Fall Processor Forum Attendee:

Welcome to Fall Processor Forum 2005. We have an outstanding program filled with the latest disclosures of new multicore technology. Also planned is an excellent seminar program. As you join us this week, there are a few points to keep in mind:

Seminars (Monday, October 24 & Thursday, October 27)
If you're registered to attend a seminar on Monday or Thursday, you will need to pick up your badge and materials the morning of your seminar in front of the Monterey Room.

FPF Expo 2005 Sponsored by IBM (Tuesday, October 25 at 5:30 PM)
Plan to attend FPF Expo 2005! At the Expo, get the latest information from the industry's leading vendors while you enjoy a delicious buffet of complimentary food and beverages sponsored by IBM.

Meals
Your registration includes complimentary continental breakfast, lunch, and break snacks on the conference and seminar days you're registered to attend. The conference-day lunches are sponsored this year by Freescale and IBM. *Important: You will need your badge to have lunch, so keep it with you at all times during the week.*

Evaluations
At the end of the forum on Wednesday, please take a moment to give us your feedback on the form provided with your conference packet. Your input enables us to continually improve and deliver high quality events most relevant to your needs.

Please wear your name badge at all times to gain admittance to the meeting rooms and meals. Conference attire is business casual; however, the temperature in the conference room may vary. Please be sure to dress appropriately. If there is anything we can do to make the conference more enjoyable or productive for you, please do not hesitate to ask a member of our forum staff.

Sincerely,

Frank Dickson
Senior Director, In-Stat

In-Stat Offices

Arizona | 6909 East Greenway Parkway, Suite 250 | Scottsdale, AZ 85254
California | 1101 S. Winchester Blvd., Bldg. N | San Jose, CA 95128
Massachusetts | 225 Wyman Street | Waltham, MA 02451
Asia-Pacific | The Signature, 51 Changi Business Park Central 2 #07-01 | Singapore, 486066
China | Room 1711 | Dacheng Plaza | 127 Xuanwumen West Street | Xicheng District | Beijing, 100031

FALL PROCESSOR FORUM

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Wednesday
October 26, 2005
Doubletree Hotel
San Jose, CA

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WEDNESDAY OCTOBER 26, 2005

9:00 AM Welcome

9:05 AM **Keynote:** *Herb Sutter, Software Architect, Microsoft Developer Division*

9:50 AM **Session Four:** Building Systems with Multicore Processors
Jim McGregor, Principal Analyst, In-Stat & Kevin Krewell, Editor in Chief, Microprocessor Report

Facing the Software Challenges of Multicore Designs
Neil Puthuff, Director of Hardware Engineering, Green Hills Software, Inc.

10:35 AM Break (20 minutes)

10:55 AM Xen and the Art of Multicore Processing
Simon Crosby, VP of Strategy & Corporate Development, XenSource

AMD "Pacifica" Technology: x86 Architectural Enhancements to Facilitate Virtualization
Kevin J. McGrath, AMD Fellow

12:15 PM **Lunch** (75 minutes)

1:30 PM Session Four continues

Useable Multicore Implementations in Embedded Applications
Toby Foster, System Architect, Freescale Semiconductor

The Power Within the Cell Processor—and How to Unleash It
Alex Chunghen Chow, Manager, S-T-I Design Center and David Krolak, Development Engineer, IBM

2:50 PM Break (20 minutes)

3:10 PM **Session Five:** High-Performance DSP
Max Baron, Principal Analyst, Microprocessor Report

StarCore V5 Architecture
Amnon Rom CTO, VP Engineering, StarCore LLC

TMS320C672x DSP for Audio Processing,
Amitabh Menon, CPU and SoC Architect, Texas Instruments

4:05 PM **Session Six:** On-Chip Interconnect for Multicore
Tom R. Halfhill, Senior Analyst, Microprocessor Report

GALS Interconnect: Delivering Transparent Connectivity for Multi-Core SoCs
Uri Cummings, VP of Product Development, Fulcrum Microsystems

Advanced Dataflow Services for Heterogeneous Multicore SoCs
Drew Wingard, CTO, Sonics

5:00 PM Adjourn

FPF 2005 Conference Program and Locations

Seminar Agenda

Monday, October 24

Implementing Low Power SoC Configurations—presented by Max Baron . . . . . .Monterey Room

Thursday, October 27

A Briefing on DSP Technology—presented by the market leaders and moderated by Max Baron . . . .Monterey Room

Seminar Schedule

7:30 AM	Registration	12:00 PM	Lunch (one hour)
8:30 AM	Seminar begins	2:40 PM	Afternoon break (20 minutes)
10:00 AM	Morning coffee break (20 minutes)	4:30 PM	Seminar ends; Q & A follows

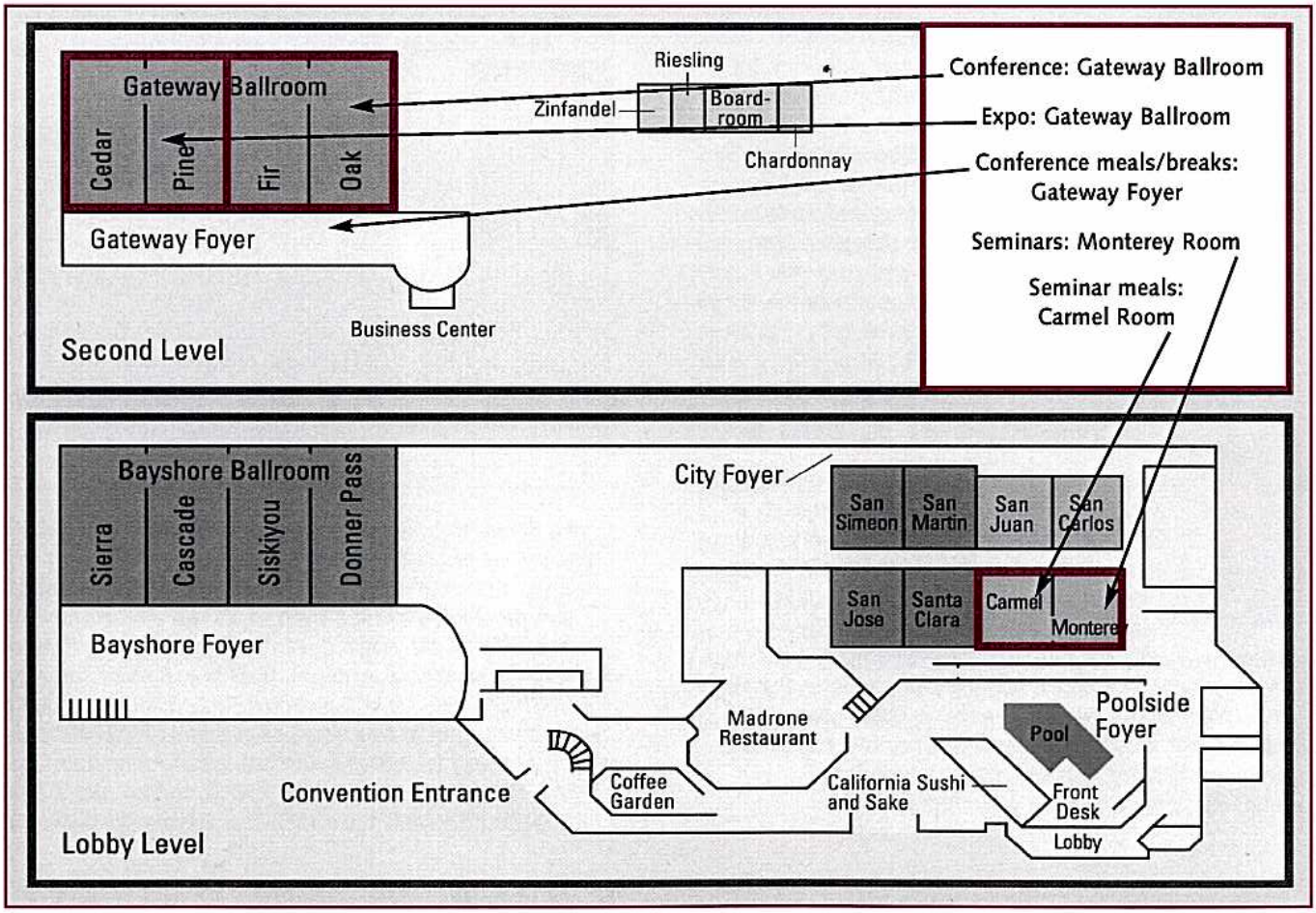
Conference Agenda

Tuesday, October 25, 2005

9:00 AM	Welcome and Introduction
9:05 AM	Keynote—Mike Fister, President & CEO, Cadence
9:50 AM	Session One—Multicore Processors
10:45 AM	Break (25 minutes)
12:25 PM	Lunch (80 minutes)
1:45 PM	Special Presentation
2:15 PM	Session Two—Innovative IP
3:10 PM	Break (25 minutes)
3:35 PM	Session Three—Processor IP for Multicore
5:30 PM	Adjourn to Expo

Wednesday, October 26, 2005

9:00 AM	Welcome
9:05 AM	Keynote—Herb Sutter, Software Architect, Microsoft Developer Division
9:50 AM	Session Four—Building Systems with Multicore Processors
10:35 AM	Break (20 minutes)
12:15 PM	Lunch (75 minutes)
1:30 PM	Session Four continues
2:50 PM	Break (20 minutes)
3:10 PM	Session Five—High Performance DSP
4:05 PM	Session Six—On Chip Interconnect for Multicore
5:00 PM	Adjourn



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FPF Conference Program

TUESDAY OCTOBER 25, 2005

9:00 AM **Welcome and Intro**
Frank Dickson, Senior Director, In-Stat

9:05 AM **Keynote:** *Mike Fister, President & CEO, Cadence*

9:50 AM **Session One:** Multicore Processors
Kevin Krewell, Editor in Chief, Microprocessor Report

A Concurrent Multi-Threaded Core for Complex SoCs
Kimming So, Senior Principal Scientist, Broadcom Corporation

SPARC64 VI/VI+: Fujitsu's Next Generation Processor
Takumi Maruyama, Manager of Enterprise Server Development, Fujitsu, Limited

10:45 AM Break (25 minutes)

The IBM PowerPC 970MP A New, Low-Power, High-Performance, Dual-Core Processor, *Norman J. Rohrer, Distinguished Engineer, IBM Corporation*

Application Customized CPU Design for Microsoft XBOX 360
Jeffrey D. Brown, Chief Engineer – Microsoft CPU Project, IBM Corporation

A Power-Efficient, Scalable Processor Family
Jim Keller, V. P. Engineering, Architecture Group, P. A. Semi

12:25 PM **Lunch** (80 minutes)

1:45 PM Special presentation: A Game Changing Innovation,
Scott Sellers, Co-founder, CTO & VP of Hardware Engineering, Azul Systems

2:15 PM **Session Two:** Innovative IP
Tom R. Halfhill, Senior Analyst, Microprocessor Report

ARM's First Low-Power Superscalar Processor
David Williamson, Co-Architect and Validation Lead, ARM

Z-Ram and the Cinderella Effect
Mark-Eric Jones, President & CEO, Innovative Silicon, Inc.

3:10 PM Break (25 minutes)

3:35 PM **Session Three:** Processor IP for Multicore
Tom R. Halfhill, Senior Analyst, Microprocessor Report

ARC's New Multi-Standard Multimedia Subsystem
Nigel Topham, Chief Architect, ARC International

High-Performance Multicore Video Decoder Technology Preview,
Gulbin A. Ezer, Hardware Design Manager, Tensilica

A Next-Generation Scalable Video Processor Core
Hans-Joachim Stolberg, CEO, videantis GmbH

5:30 PM Adjourn to Expo

FALL PROCESSOR FORUM
www.in-stat.com/fpf

FPF 2005

San Jose Doubletree
October 25 – 26, 2005

FPF 2005 Session Leaders

Welcome and Intro

Frank Dickson is senior director of In-Stat's semiconductor and convergence groups. Dickson's roles include business operations of Spring Processor Forum, Fall Processor Forum, and Microprocessor Forum Japan. Previously, Dickson was publisher of *Microprocessor Report*, senior director of sales and marketing for In-Stat and principal analyst for In-Stat's Semiconductor Market Services. Prior to joining In-Stat, Dickson was a product manager and business analyst with SpeedFAM, a semiconductor capital equipment company located in Chandler, AZ.

Session 1

Kevin Krewell is editor in chief of *Microprocessor Report* and author of the 2003 edition of the Intel Microprocessors Service. He is a 25-year veteran of the electronics industry with specific experience in x86 and RISC processors, computer-graphics displays, military-related DSPs, technical marketing, and applications engineering. Krewell joined MDR after spending over 10 years at Advanced Micro Devices, where he served in technical marketing and field application-engineer roles.

Sessions 2, 3, and 6

In 2002, **Tom R. Halfhill** rejoined In-Stat as a senior analyst after working as a technical analyst and writer for ARC Cores. Previously, during 1999-2000, he was a microprocessor analyst for MicroDesign Resources. Halfhill has been a journalist since 1977 and has covered technology since 1982. He was a senior editor at BYTE Magazine for six years, where he wrote nearly 200 articles about microprocessors, Java, thin-client computing, computer reliability, data compression, broadband communications, and many other topics.

Session 4

Jim McGregor has rejoined the In-Stat team as a principal analyst and editor. He was the principal analyst for the In-Stat DRAM service from 1994 to 1997. McGregor joined STMicroelectronics' New Ventures Group in 1997, aiding in the introduction of new embedded processors, graphics processors and biometric sensors, and in 1999, he joined Motorola to assist in the launch and branding of ON Semiconductor, a spin-off of Motorola's Semiconductor Components Group. McGregor rejoined Motorola in 2000, driving new system products and market strategies for the Motorola Computer Group. In addition to his business and marketing experience, he has an engineering background in both the semiconductor and embedded systems realm.

Session 5

Max Baron serves as principal analyst and senior editor of *Microprocessor Report*, In-Stat's award-winning newsletter. Max Baron comes to *Microprocessor Report* and the forum group from In-Stat, where he was principal analyst for the Micrologic Information Service, covering microprocessors, microcontrollers, and DSPs. A 35-year veteran of the electronics industry, Baron's prior experience includes designing microprocessors and embedded systems, primarily as an R&D manager at companies including National Semiconductor, Sun Microsystems, Sun Microelectronics, and Fujitsu Microelectronics.

Speaker Biographies

Day One — October 25

Tuesday Keynote: Mike Fister is president and chief executive officer of Cadence Design Systems, Inc. Before joining Cadence, he spent 17 years at Intel Corporation, where he was most recently senior vice president and general manager of the company's Enterprise Platforms Group.

Previously, Fister served as vice president and general manager of the performance microprocessor group, where he managed Intel's IA-32 processor development organization. He was also responsible for the design, development and marketing of IA-32 processors, including the last versions of the Intel486 and the entire line including the Pentium Pro, Pentium II, Pentium III, Celeron, Pentium II Xeon, and Pentium III Xeon processors.

Fister is a graduate of the University of Cincinnati where he received B.S. and M.S. degrees in electrical engineering in 1977 and 1978 respectively.

Session One

Kimming So is the architect of the Embedded Processor Technology in the Communication Broadband Group at Broadcom Corporation. Prior to Broadcom, he was the architect of the Embedded System Group at Philips Semiconductors. Before that, he was with the IBM T.J. Watson Research Center performing research on computer architecture, memory hierarchy and multiprocessor systems, and he was the architect of a PowerPC multiprocessor system.

Takumi Maruyama is a manager of processor development department 1, at Fujitsu. His recent interests include microprocessor architecture and VLSI design. Since he joined Fujitsu in 1986, he was involved in the development of Fujitsu K business servers for several years. He started working on the first SPARC64 processor design in 1993 and was involved in the development of the SPARC64 GP processor of Fujitsu GRANDPOWER/PRIMEPOWER unix servers. Maruyama has worked on SPARC64 VI development since 2001. He holds a B.E. in mathematical engineering and instrumentation physics from the University of Tokyo.

Norman Rohrer is a senior technical staff member in the PowerPC microprocessor group within the system and technology group of IBM, located in Essex Junction, VT. Rohrer received his B.S. in physics and mathematics from Manchester College, North Manchester, IN, in 1987. He received his M.S. and Ph.D. in electrical engineering from the Ohio State University, Columbus, OH in 1990 and1992, respectively. His interests lie in the area of high-speed circuit optimization for future technologies. Rohrer holds 17 patents and is a co-author on two books titled *High Speed CMOS Circuit Design Styles* and *SOI Circuit Design Concepts*.

Jeffrey Brown is the chief engineer for the XBOX360 CPU chip development. He is an IBM distinguished engineer in the engineering & technology services division of IBM and a member of the IBM Academy of Technology. He has been part of E&TS from its inception and has a 15 year history of CPU, memory, and IO subsystem development for iSeries, pSeries, and xSeries within IBM.

Jim Keller has distinguished himself over his 24-year career, through his contributions to the architecture of several pivotal processors, including the DEC Alpha 21164 and 21264 as well as AMD's Opteron. Prior to P. A. Semi, Keller served as the director of architecture for the SiByte group at Broadcom, where he architected the BCM1400 and follow-on processors. Keller co-authored the HyperTransport and x86-64 specifications and holds over 100 patents.

Special Presentation: Scott Sellers, with leadership in building and delivering advanced hardware, leads the development of Azul Systems chip architectures. Prior to Azul, Sellers founded 3dfx Interactive, a graphics processor company. He served at 3dfx as VP of engineering, CTO and a member of the board of directors and delivered seven award-winning products.

Session Two

David Williamson is a consulting member of technical staff at the ARM Austin Design Center. He is currently the lead for both the microarchitecture performance evaluation and validation of the Cortex A8 microprocessor. He was also one of the chief architects responsible for defining the microarchitecture of this processor. Before working on the Cortex A8, he was a key contributor in designing the ARM10 family of processors. Prior to joining ARM, Williamson worked at AMD on the design of the Athlon processor. He received his B.S.E.E. and M.S.E. from the University of Illinois at Urbana-Champaign.

Mark-Eric Jones joined Innovative Silicon, a semiconductor memory technology company, as CEO in August 2004. Previously, he was vice president and general manager at MoSys, Inc. in Sunnyvale, California, responsible for building the memory technology Intellectual Property (IP) licensing business. Jones has served as president of the board of RAPID, the semiconductor IP trade association. He has an M.A. degree in electrical sciences from Trinity College, University of Cambridge, UK.

Speaker Biographies

Day One Continued — October 25

Session Three

Nigel Topham is chief architect for ARC International and professor of computer systems at the University of Edinburgh. He has led a number of processor design teams, including the ARC 600. Prior to joining ARC, he was chief architecture for Siroyan, a startup that created a high-performance, scalable VLIW DSP. He is a founding director of the Institute for Computing Systems Architecture at Edinburgh University, where he also teaches computer architecture to the next generation of processor architects.

Gulbin A. Ezer is a hardware design manager at Tensilica Inc., working on configurable and extensible processor technologies. She has extensive industry experience in the architecture and design of dataflow supercomputers (Cydrome Inc.), workstations (MIPS Inc.), general purpose and multimedia processors (SGI Inc.). Ezer holds three patents in multimedia processor design. She has a B.S. degree in electrical engineering from Yale University and an M.S. degree in electrical and computer engineering from University of California, Santa Barbara.

Hans-Joachim Stolberg received the Dipl.-Ing. E.E. degree from U Hannover, Germany, in 1995. He was with NEC Corp., Japan, in 1995-1996 and with TiTech, Japan, in 2001. From 1996-2004, he was a staff member and chief architect with U Hannover. Since 2004, Stolberg co-founded videantis GmbH and is its CEO and CTO.

Day Two — October 26

Wednesday Keynote: Herb Sutter is a software architect in Microsoft's developer division. He is the author of four books and hundreds of technical articles and papers about software development, including the widely read "The Free Lunch Is Over" article that first identified and coined the term "concurrency revolution." Sutter also serves as chair of the ISO C++ standards committee.

Session Four

Neil Puthuff is director of hardware engineering for Green Hills Software, Inc. He has more than 20 years of engineering experience, and several US patents awarded or pending.

Simon Crosby joins XenSource from Intel, where he was a principal engineer leading strategic research in distributed autonomic computing, platform security and trust. Previously, Crosby founded CPlane Inc., a network optimization software vendor. Prior to CPlane, he was a tenured faculty member at Cambridge University, UK, where he led research network performance and control and multimedia operating systems. Crosby is the author of over 35 research papers and patents.

Kevin J. McGrath is a fellow at AMD, California microprocessor division. He is the architect of AMD's 64-bit extensions and currently manages the AMD64 architecture and RTL team. McGrath's work experience includes 20 years in CPU design and verification, first for Hewlett-Packard and later for ELXSI. His career eventually brought him to AMD, where he has worked on the microarchitecture for the Nx586, AMD-K6(r), and AMD Athlon(tm) processors, leading the microcode teams for those projects. McGrath has a bachelor's degree in engineering technology from California Polytechnic University, San Luis Obispo.

Toby Foster is a system architect for Freescale's network computing and systems group, focusing on the development of high-performance PowerPC processors. He also has held roles as system architect and applications engineering manager for Freescale's network processors. Foster holds an M.S. and B.S. in electrical engineering from Harvey Mudd College.

Alex Chunghen Chow is a senior programmer and a software development manager in IBM's Cell Processor Design Center (Austin, TX). He leads a team developing kernel, tools, workloads, libraries, demo, and samples for the Cell processor chip bring-up. Chow received B.S. and M.S. degrees in electronic engineering from National Chiao-Tung University, Taiwan. He also received a Ph.D. degree from the University of Arizona in electrical and computer engineering. His fields of work include discrete event simulation, distributed and parallel simulation/programming, and object-oriented programming and framework.

David J. Krolak is a senior engineer in the engineering and technology services division at IBM. He received a B.S degree in electrical engineering from the University of Wisconsin at Madison in 1979. In his 25 years at IBM, Krolak has worked on DRAM controllers, was the lead designer for the L2 cache controllers used in the RS/6000 S70, S80 and S85 models, and is the lead designer of the Element Interconnect Bus used in the Cell chip. He holds nine patents and is currently working on future Cell designs.

Speaker Biographies

Day Two Continued — October 26

Session Five

Amnon Rom was named vice president of research and development and chief technology officer of StarCore LLC in September 2002. Rom also serves as the general manager of StarCore's subsidiary design center in Tel Aviv, Israel. Rom has 16 years of professional R&D experience in the technology industry in both engineering and management capacities. Prior to joining StarCore, Rom served as vice president of R&D for Infineon's Tel-Aviv Design Center for seven years. In that role, he was also the chief architect of the Carmel DSP 10xx. Prior to joining Infineon, Rom spent 10 years in various technical and management positions at National Semiconductor and at DSP group where he was a senior engineer on the team that developed the "Oak" DSP core. Rom earned a B.S.C. degree from the electrical engineering Faculty, Tel Aviv University. He also holds an M.B.A. degree in industrial management from the Technion, Haifa.

Amitabh Menon is a CPU and SoC architect at Texas Instruments. Menon has been with TI since 1995. Originally in DSP product development in Bangalore, India, since 2004 he has worked as an SoC architecture technology manager in Texas, focused on advanced architecture and chip technology. He has a bachelor of technology degree from Mangalore University, graduating "First Class with Distinction." He earned an M.S. with the Indian Institute of Science in 2001. Menon is "Member, Group Technical Staff, Semiconductor Group" on the Texas Instruments Technical Ladder since 2001.

Session Six

Uri Cummings is the co-founder and vice president of product development at Fulcrum Microsystems. While a student at Caltech, Uri conducted advanced research both in the areas of optical component design and asynchronous circuit design. In January 2000, Cummings co-founded Fulcrum Microsystems with Andrew Lines to commercialize their joint research in asynchronous design and became the company's president and CEO. In April 2001, he recruited Bob Nunn to replace him as president and CEO, and returned to his strengths as VP of product development. Cummings has a B.A. degree in English from Wesleyan University ('94), a B.S. degree in electrical engineering from Caltech ('94), and an M.S. degree in electrical engineering from Caltech ('95).

Drew Wingard is a founder and the chief technical officer of Sonics, Inc., which has been providing SMART interconnects since 1999. He was the original architect of Sonics' SiliconBackplane and creator of the Open Core Protocol specification. He currently represents Sonics on the Governing Steering Committee of OCP-IP, where he chairs the specification working group. Prior to founding Sonics, Wingard led the development of advanced circuit and CAD methodology for MicroUnity Systems Engineering, Inc. Previously he had cofounded Pomegranate Technology, where he designed an advanced SIMD multimedia processor. He received a B.S. from the University of Texas, Austin, and an M.S. and Ph.D. from Stanford University, all in electrical engineering. While at Stanford, Wingard's research explored the optimization of design processes between architectural, logical, circuit, and physical design with an emphasis on tools and automation.